## REMARKS

Applicants thank Examiner for their detailed review of the application.

The Office Action reiterated a request that Applicants add a "Brief Summary of the Invention" description to the application under 37 CFR 1.77(b). Examiner stated that the language *when set forth* in 37 C.F.R. §1.73 is not conditional language. However, applicants respectfully submit that the phrase *when set forth* implies that there are occasions within an application that the brief summary of invention may not be set forth. For instance, if a brief summary invention must be included or is to be always included according to 37 C.F.R. §1.73, then 37 C.F.R. §1.73 would only need to say that the summary should be commensurate with the invention..." In contrast, the phrase *when set forth* implies only when a brief summary of invention is included should it be commensurate with the invention. Hence a brief summary of invention is not necessarily required, but is only to be commensurate with the invention, when set forth. Therefore, applicants respectfully request that the application is in condition for allowance without including a "Brief Summary of the Invention."

Examiner objected to Figure 9, as it was not commensurate with the disclosure. Applicants have submitted herewith a replacement drawing sheet for Figure 9. The copied contents from block *910* into block *915* have been replaced by the disclosure in the specification at page 17 in paragraph 0050, "In addition, as shown in block *915*, the target SMBase may be restored to targeting the first processor's SMBase address."

Examiner objected to claims 31, 37, 38, 42, and 58 due to informalities. Claim 31 has been amended to correct the antecedent basis, now including "executing the SMI handler to handle the SMI for the second processor." Claim 36 has been amended to depend from claim 35 instead of claim 33. Therefore, Claim 37's reference to the first SMBase address has proper antecedent basis.

Claim 38 has been amended to provide antecedent basis for "a target SMBase," and to remove the reference to "the SMI handler." Claim 42 has been amended to reference, "the first memory location," instead of the first memory address. Claim 58 has been amended to include a target SMBase referenced by the SMI code."

Examiner objects to claims 2, 3, 8, 9, and 11 under 35 U.S.C. 112 as they refer to the second processor. Independent claim 1 has been amended to remove the reference to two "a second processor" occurrences having amended line 6 to "the second processor."

Examiner rejects claims 1, 3-5, 12-14, 18, 22, 23, 45, and 47-49 under 102(a) as being anticipated by Dale (GB 2382180A).

Applicant's claim 1 includes, "the wake-up signal references a first memory address of a default SMI handler." Dale does not disclose referencing a first memory address of a default SMI handler. In fact, Dale's RF_RADIO_ON signal is merely a voltage logic signal set by GSM ULPD. Furthermore, the RF_RADIO_ON signal is provided to GPIO unit 321, which generates the interrupt to the MMI processor. (See page 18 lines 26-28.) Dale further states that, "the MMI processor recognises the interrupt as originating from the GSM sub-system and initiates the wake up process." However, there is no suggestion or reference in Dale that either the RADIO_ON signal or the interrupt generated by the GPIO unit references a memory address of a default SMI handler. As claims 2-11 depend from claim 1, applicant respectfully submits that claims 2-11 are in condition for allowance for at least the same reasons stated above.

Applicant's claim 12 includes executing code at a first memory location with a first processor and executing the code from the first memory address with the second processor. Dale merely discloses the use of a memory, i.e. memory 350 of Fig. 3. However, Dale does not disclose executing code from the same location within memory 350. In fact, applicants disclose the

advantage of executing a single default SMI handler/code by both processors to save memory space at page 18 paragraph 0052, which is not addressed or contemplated in Dale's disclosure. Similarly, applicant's claim 45 includes, "the first processor executes the code at the first memory address...," and "the second processor executes the code at the first memory address." Therefore, applicant respectfully submits that claims 12 and 45 are in condition for allowance, as well as their dependent claims 13-25 and 46-53, for the reasons stated above.

Examiner rejects claim 40 under U.S.C. 103 as being unpatentable over Dale in view of Nalawadi (US 2003.0009654 A1). However, claim 40 has been amended to include the same limitation of claim 1, i.e. "wherein the wake-up signal references a first memory address of a default SMI handler." As Nalawadi does not disclose the wake-up signal references a first memory address of a default SMI handler and Dale does not disclose the limitation, as discussed above, applicant respectfully submits that claim 40 and its dependent claims 41-44 are now in condition for allowance for the same reasons as state above in reference to claim 1 and its dependent claims.

Next, Examiner rejects applicants 26-33, 35-38, 54-59, and 61 under 35 U.S.C 102(b) as being anticipated by Nguyen et al. (US 2002/0099893).

Nguyen et al. discloses in paragraphs 0019 to 0019 the following:

In one example, processor 12b is the processor that issued the software instruction that caused the issuance of the software SMI. The software SMI signature is saved to the SMRAM space 82 associated with processor 12b. *In this example, processor 12c has been selected as the processor whose SMI handler will address the software SMI.* Once processor 12c locates the software SMI signature 88, which in this example is in the SMRAM space 82 associated with processor 12b, the SMI handler of processor 12c uses the parameters that have been passed to the SMRAM that includes software SMI signature. The parameter passing step 54 of FIG. 2 is accomplished through the SMRAM space of the processor that caused the initiation of the software SMI, without regard to the processor that is selected by the BIOS of the computer system to handle the software SMI.

[0019] In some cases, only one of the processors of a multiprocessor system is designated as being the processor that handles all system management interrupts. In this scenario, only one processor of the computer system, the SMI processor, will include a SMI handler and the responsibility for handling all system management interrupts will be passed to this processor.

(emphasis added).

Here, Nguyen discloses a method of passing parameters to a single processor executing an SMI handler. As noted, processor 12c is selected as the processor whose SMI handler will address the software SMI. Processor 12b is merely the processor that issued the initial instruction causing the generation of an SMI to be handled. Moreover, later Nguyen discloses that one processor may be dedicated as the processor to handle all SMIs, which entails only one processor executing SMI handler code. In contrast, applicant's claims 26, 32, and 54 include limitations similar to executing a SMI handler or SMI code on a first processor and executing the SMI handler or the SMI code on a second processor. Unlike execution of SMI code on one processor with parameter passing from other processors, applicant's claims include execution of the SMI handler or SMI code on both the first and the second processor. Therefore, applicants respectfully submit that claims 26, 32, and 54, as well as their dependent claims 27-31, 32-39, and 55-61, are now in condition for allowance for the reasons stated above.

Consequently, Applicants respectfully submit that claims 1 - 61 are now in condition for

allowance.

Respectfully submitted,

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David P. McAbee
Reg. No. 58,104

12400 Wilshire Blvd.
Seventh Floor
Los Angeles, CA 90025-1026
(408) 720-8300